22.2 Statistical Characterization and On-Chip Measurement Methods for Local Random Variability of a Process Using Sense-Amplifier-Based Test Structure

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Measurement, characterization, and estimation of local random variation in threshold voltage (V_t) are crucial for yield learning/enhancement in nanoscale technologies, particularly for characterization of area-constrained circuits, such as SRAM cells. Conventionally, local random mismatch is characterized by measurement of current difference between identical neighboring devices, followed by complex data analysis to extract Vt difference from current difference [1-3]. This paper demonstrates a sense-amplifier-based test circuit and measurement method for on-chip characterization of local random variation. Instead of complex and sophisticated analog voltage-current measurements required in conventional schemes, we use a simple digital measurement technique. Moreover, this method directly characterizes the complete probability distribution of local mismatch, thereby eliminating the need of complex data analysis. Further, using the digital nature of the measurement, we propose a built-in-self-test scheme for on-chip measurement of device mismatch, which significantly reduces characterization time and cost.

The test circuit is based on a current latch-type sense amplifier (CLSA) shown in Fig. 22.2.1. Monte-Carlo simulations show that the offset voltage (minimum V_{IN}-V_{INB}) required for correct sensing of a CLSA strongly depends on local random V_t variation while systematic (correlated) variation has minimal effect. The offset voltage is a linear combination of the offset due to V_t mismatch in the driver MOSFETs (N_{DR}-N_{DRB}, $V_{os\text{-}driver}$) and the mismatches in the latch MOSFETs (P_{INV}-N_{INV}, P_{INVB}-N_{INVB}, $V_{os\text{-}latch}$). Although, $V_{os\text{-}driver}$ depends only and directly on the mismatch between the driver MOSFETs (independent of the strength of the other devices), $V_{os\text{-}latch}$ depends on the strength of the latch MOSFETs and the clock MOSFET (N_{Clk}). The test circuit uses the driver transistors as the device under test *(DUT)* and the offset voltage of the CLSA as a measure of the V_t mismatch. Hence, $V_{os\text{-}driver}$ directly measures the local V_t mismatch, while $V_{os\text{-}latch}$ introduces error. $V_{os\text{-}latch}$ is minimized by reducing the strength of the clock transistor, increasing the size of the latch NMOS and PMOS (keeping the NMOS to PMOS beta ratio high, ~8), and increasing the rise time of the sense-amplifier enable signal (SAE) [4].

The complete test-structure contains an array of CLSAs optimized to reduce $V_{os\text{-}latch}$. Driver FETs (DUTs) are placed in closest possible proximity. The inputs (V_{IN}, V_{INB}) of all CLSAs in a column are shared. Row and column decoders select each CLSA for offset measurement. The SAE signal for the unselected rows and inputs of CLSAs in the unselected columns are gated to '0' to prevent spurious switching of all unselected CLSAs. To measure the offset voltage, we select a CLSA and vary Δ ($V_{IN} = V_{TEST}$, $V_{INB} = V_{TEST} \pm \Delta$). The digital output of the selected CLSA is scanned to determine the minimum Δ required for correct sensing ('1'-'0' or '0'-'1' transition), which indicates the V_t mismatch.

Since the test circuit requires only application of analog voltage difference and measurement of a digital output, it can be used to design a completely on-chip built-in-self-test circuit for random variability measurement (Fig. 22.2.1). An on-chip controller selects a sense-amplifier, applies different Δs (generated by a voltage divider network) and scans the digital output to measure its offset voltage. The final (digitized) Δ value is stored in an on-chip memory.

To confirm the operation of the circuit, we estimate the offset voltage (i.e., V_t mismatch) distribution using Monte Carlo simulations by randomly applying V_t shifts to all the transistors in the test circuit (assuming area-dependent variations for V_t). Simulation in predictive 70nm technology [5] shows close match between the estimated (through offset voltage measurement) and applied Vt mismatch distribution with 5 to 8% error in prediction of standard deviation and complete distribution (Fig. 22.2.2). Reduction of V_{TEST} helps to improve estimation accuracy as it reduces the current through the clock transistor (lower latch offset). Next, we estimate the offset distribution considering *total* random variation in a process and applied it as V_t variation to obtain the distribution of a specific circuit parameter. Simultaneously, we also obtain the true distributions of that parameter by directly applying the total variation. Simulation results in Fig. 22.2.3 show that the test circuit can accurately predict the true current mismatch between identical transistors (0.13µm CMOS, hardware calibrated process variation parameters) and true read/trip voltage distribution in an SRAM cell (predictive 70nm technology, random L and V_t mismatch). The estimated offset distribution closely predicts the total random mismatch and can be used as V_t mismatch for circuit simulation. We observe that ~200 test-structures are sufficient to predict standard deviation within 10% error with a 95% confidence level and minimum resolution of 10mV in steps of Δ provides good accuracy (Fig. 22.2.3).

A testchip is fabricated in 0.13µm triple-well bulk-CMOS and measured to show the operation of the structure (Fig. 22.2.7). An array of 512×16 CLSA structure with DUTs of different geometry and V_ts is designed and accessed using a 5b row and 4b column decoder (Fig. 22.2.4). All NMOS devices, except DUTs, are placed in an isolated p-well. The digital nature of the test circuit allows software-controlled automated measurement of local mismatch. Measurements are performed at V_{DD} = 1.5V, V_{TEST} = 1.0V and clock period of 300µs. Fig. 22.2.4 shows that the measured offset voltage for different CLSAs for a particular die are random and local in nature. The V_t mismatch distribution for minimum size devices is close to normal (Fig. 22.2.5). Increasing the widths of DUTs reduces the spread in the mismatch (Fig. 22.2.5). The standard deviation, σ, of V_t mismatch obtained from different dice are similar. Moreover, the σ values for different widths tend follow the characteristics $W^{-1/2}$ nature expected for V_t mismatch due to random dopant fluctuation ([6], Fig. 22.2.6). However, the presence of area independent mismatch is also observed—σ reduces at a rate slower than $W^{-1/2}$. V_t mismatch is larger for higher V_t devices, because higher doping tends to increase the RDF effect [6], and smaller for longer channel devices, because of larger channel area and less short channel effect. The measurement results show that the proposed test structure extracts local random mismatch in a process with very low test time and cost and makes the design of an on-chip built-in-self-test scheme feasible. Such a scheme is very useful for fast and accurate characterization of process which will facilitate technology development and help make pre-silicon design decisions to improve circuit robustness in nanometer technologies.

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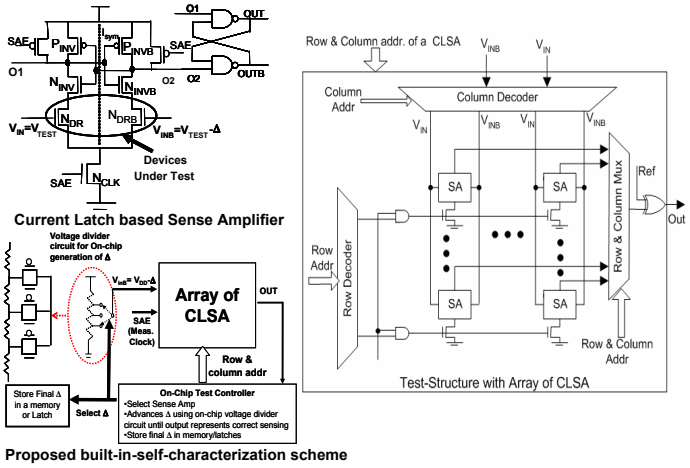

Figure 22.2.1: The test-structure and on-chip local variability measurement system.

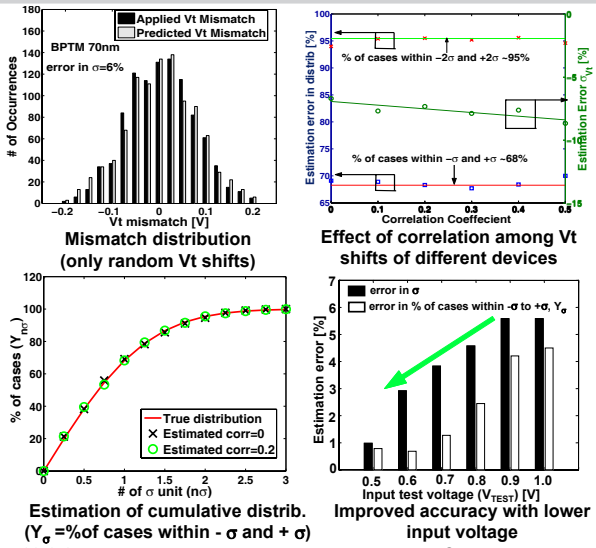

Figure 22.2.2: Verification of the test structure using Monte-Carlo simulations in predictive 70nm technology.

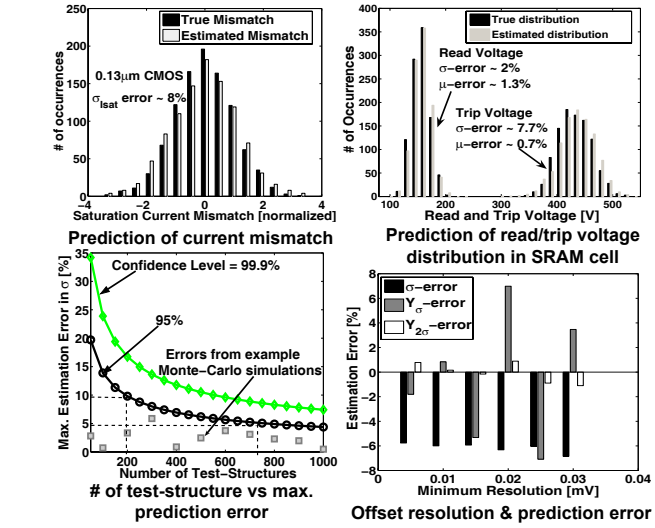

Figure 22.2.3: Effectiveness and requirements of the test structure (Monte-Carlo simulation results in predictive 70nm technology).

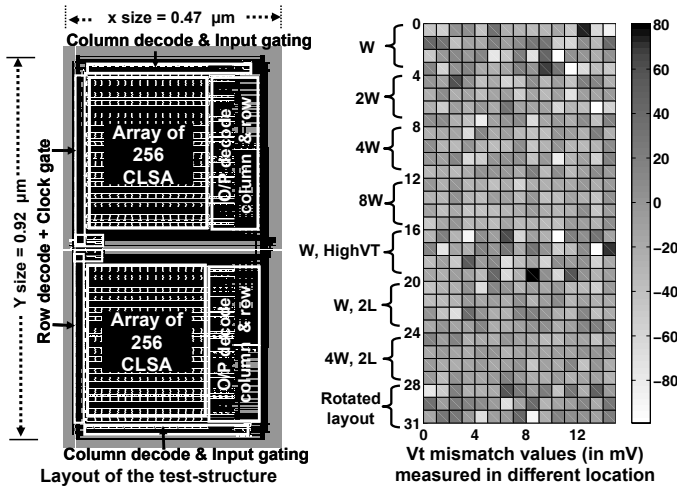

Figure 22.2.4: Measured values of local random mismatch in different locations of a die (130nm CMOS technology).

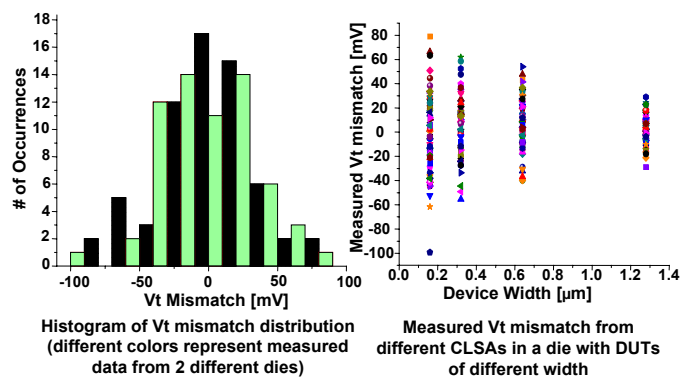

Figure 22.2.5: Measured values for V_t mismatch distribution and the effect of device width on mismatch distribution (130nm CMOS technology).

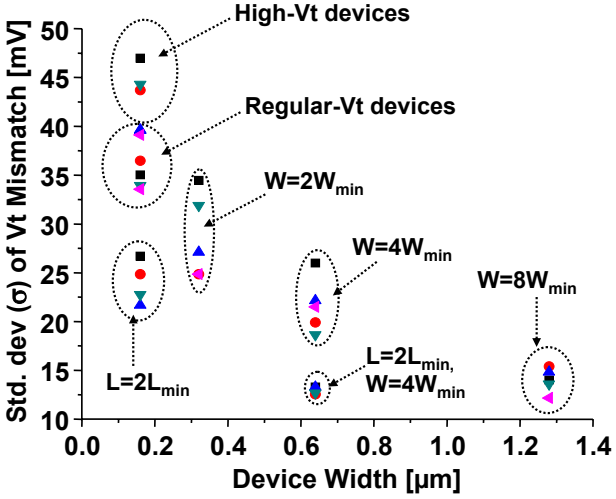

Figure 22.2.6: Impact of device width and threshold voltage on standard deviation of V_t mismatch (Measured results from 5 different dies in 130nm CMOS technology).

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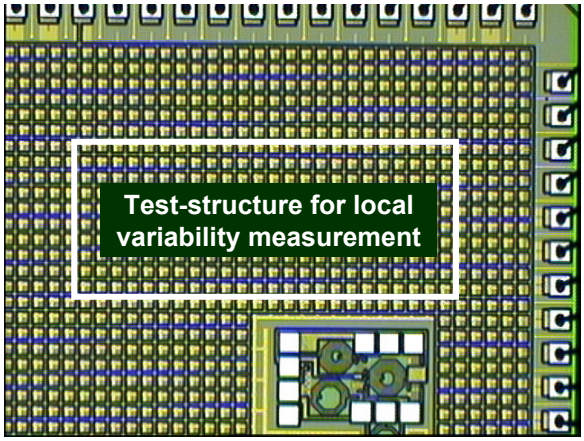

Technology: 130nm bulk-CMOS,triple-well dual Vt
Measurement conditions: V_{DD}=1.5V, V_{TEST}=1.0V,
External clock frequency = 3.33kHz
(period=300µs, with 50% duty cycle)

Figure 22.2.7: Partial die photo showing the test-structure.

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